CLAIMS

1. A driver, comprising:

a battery terminal (18) and a ground terminal (14) for connection to a voltage battery output and a ground battery output, respectively;

an output terminal (16) for driving a coil (92);

an energise FET (4) having a source (42), a gate (48) and a drain (46);

a control FET (6) having a source (62), a gate (68) and a drain (66); and

a freewheel FET (8) having a source (82), a gate (88) and a drain (86),

wherein the energise FET is connected with source and drain between the output terminal (16) and the ground terminal (14), and the control FET (6) and freewheel FET (8) are connected in series between the battery terminal (18) and the output terminal (16), the sources and drains (62,66,82,86) of the control and freewheel FETs (6,8) being arranged reversely so that current flowing through the control and freewheel FETs (6,8) in series flows from source to drain in one of the control and freewheel FETs (6,8) and from drain to source in the other.

2. A driver according to claim 1, wherein the source (42) of the energise FET (4) is connected to the ground terminal (14) and the drain (46) is connected to the output terminal (16);

the drain (66) of the control FET (6) is connected in common with the drain (46) of the energise FET (4) to the output terminal (16); and

the drain (86) of the freewheel FET (8) is connected to the battery terminal (18) and the source (82) is connected to the source (62) of the control FET (6).

3. A driver according to claim 1 or 2 comprising a common semiconductor substrate (3), wherein the drains (46, 66) of the control FET (6) and the energise FET (4) are formed in the common semiconductor substrate and the drain (86) of the freewheel FET (8) is isolated from the common semiconductor substrate.

4. A driver according to claim 3 further comprising control circuitry (10) integrally formed in the common semiconductor substrate (3), the control circuitry (10) having a high voltage power rail (52) connected to the battery terminal (18) and a low voltage power rail (54) connected to the ground terminal (14) for powering the control circuitry from the battery and ground terminals.

5. A driver according to claim 4 wherein the control circuitry includes:

high-side control circuitry (58) integrated in the common semiconductor substrate and connected to the gates (68, 88) of the control and freewheel FETs (6, 8) to control the FETs; and

low-side control circuitry (56) integrated in the common semiconductor substrate and connected to the gate (48) of the energise FET (4) to control the energise FET.

6. A driver according to claims 4 or 5, wherein the control FET (6) is arranged to have a higher gate capacitance than the freewheel FET (8), and the control circuitry is arranged to turn the control FET (6) fully on in the energise mode and, on switching from the energise mode to the freewheel mode, to connect the gates of the freewheel FET (8) and the control FET (6) together.

7. A driver according to any of claims 4 to 6 wherein the control circuitry (10) further comprises temperature and voltage overload protection (59) for protecting one or more of the energise FET, the control FET and the freewheel FET.

8. A driver according to any of claims 4 to 7 wherein the control circuitry is arranged to switch the FETs between an energise mode in which the energise FET is on and the freewheel FET is off, a freewheel mode in

which the energise FET is off and both the control and freewheel FETs are off and a ring-off mode in which the energise FET is off and the control FET is off.

9. A driver according to any of claims 3 to 8 wherein the freewheel FET (8) is a discrete FET formed in a separate semiconductor substrate.

10. A driver, comprising:

a battery terminal (18) and a ground terminal (14) for connection to a voltage battery output and a ground battery output, respectively;

an output terminal (16) for driving a coil;

high and low side driver FETs (4, 6) integrated in a common substrate (3) and connected between the battery terminal (18) and the output terminal (16) and the ground terminal (14) and the output terminal (16), respectively;

high-side control circuitry (58) capable of operation when the voltage on the common substrate is at least 1V above the voltage on the ground terminal integrated in the common semiconductor substrate, the high-side control circuitry being connected to the gates of the high side driver FET or FETs to control the high side driver FET or FETs; and

low-side control circuitry (56) capable of operation even when the voltage on the common substrate is close to the voltage on the ground terminal integrated in the common semiconductor substrate, the low-side control circuitry being connected to the gates of the low side driver FET or FETs to control the low side driver FET or FETs.

11. A driver according to any preceding claim wherein the FETs (4, 6) are each n-type.

12. A coil control circuit, comprising:

a driver (2) according to any preceding claim;

a battery (90) having a voltage battery output connected to the battery terminal (18) of the driver and a ground battery output connected to the ground terminal (14) of the driver; and

a coil (92) connected between the output terminal (16) of the driver and the voltage battery output.

13. A coil control circuit according to claim 12 wherein the coil (92) is a solenoid actuator having a mechanical actuator actuated by current in the coil.

14. A method of operation of a coil control circuit, comprising:

providing a coil control circuit having a coil (92), a battery (90) having positive and negative outputs, and a driver (2), the driver having an output terminal (16) connected through the coil (92) to a first one of the battery outputs, an energise FET (4) connected between the output terminal (16) and the other one of the battery outputs; and control (6) and freewheel (8) FETs of the like conductivity type connected reversely in series between the output terminal and the first one of the battery output;

switching to an energise mode in which the energise FET (4) is on and the freewheel FET (8) is off to energise the coil;

switching to a freewheel mode in which the energise FET (4) is off and both the control (6) and freewheel (8) FETs are on to retain the coil energised; and

switching to a ring-off mode in which the energise FET (4) is off and the control FET (6) is off to de-energise the coil.

15. A method according to claim 14 further including switching the control FET (6) fully on in the energise mode and, on switching to the freewheel mode from the energise mode, connecting the gates of the freewheel (8) and control (6) FETs together to share charge to switch on the freewheel FET (8).